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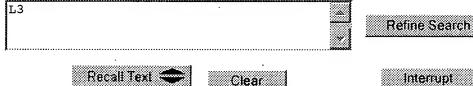
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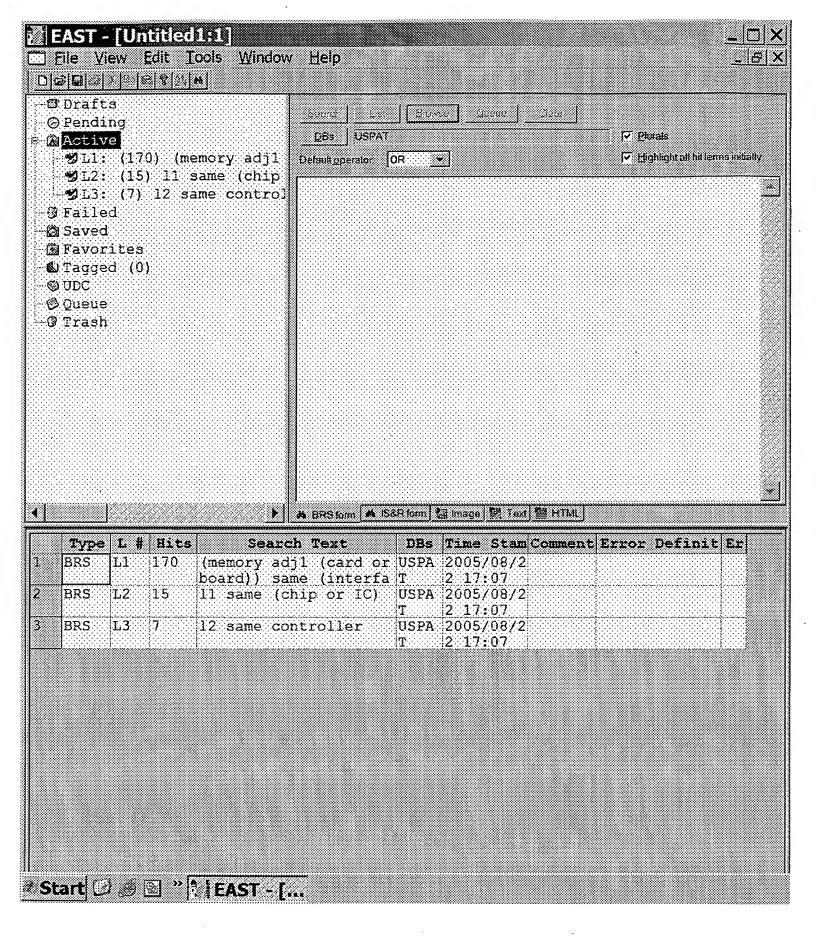
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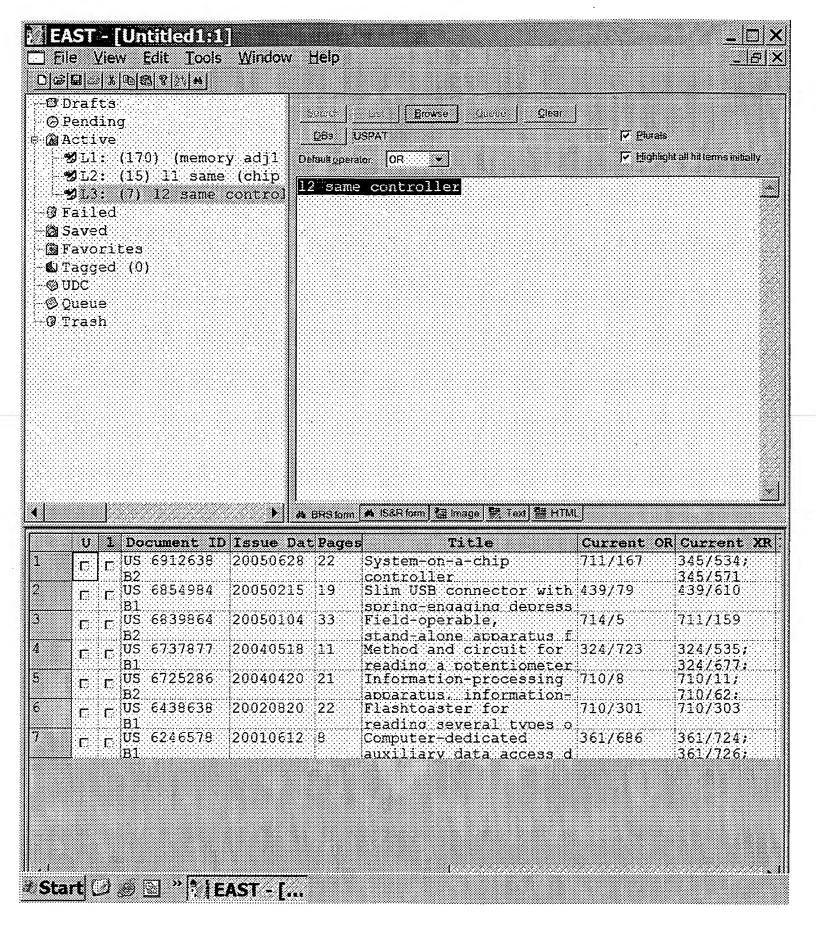
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<u>L3</u>	L2 same controller	, 136	<u>L3</u>
<u>L2</u>	L1 same (chip or IC)	nonial 75	<u>L2</u>
<u>L1</u>	L1 same (chip or IC) (memory adj1 (card or board)) same (interfac\$3 near5 (USB or "universal sexail bus"))	879	<u>L1</u>

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2. Memory on the move

Sherwin, R.M.;

Spectrum, IEEE

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solution with double FIFO buffers The performance improvement of a photo card reader by the use of a high-integration chip

Ying-Wen Bai Chang-Chih Liu

Dept. of Electron. Eng., Fu Jen Catholic Univ., Taipei, Taiwan

This paper appears in: Consumer Electronics, IEEE Transactions on

Publication Date: May 2005

On page(s): 329 - 334 Volume: 51, Issue: 2

INSPEC Accession Number:8507897

Digital Object Identifier: 10.1109/TCE.2005.1467967

Posted online: 2005-07-18 08:16:37.0

the SDRAM operation to increase the amount of the memory bandwidth. Second, we use a dual port design of the SDRAM with a double from the previous system. Our new design has an improvement in the processing speed of about 4.4 times for displaying photos module to increase the usage efficiency of the bandwidth. Using the extra gate counts of double FIFO buffers results in an increase of 3.3% buffer for the strip module to increase the usage efficiency of the bandwidth. Third, we also use a double buffer for the mem/spl l.bar/ctrl previous design of the photo card reader. In this paper, we propose three ways to overcome this drawback. First, we double the clock rate of The insufficient bandwidth of SDRAM access has created a bottleneck in the performance of displaying and processing when used in

index Terms

Controlled Indexing

SRAM chips buffer storage digital photography memory cards smart cards

SDRAM clock rate double FIFO buffer dual port design high-integration chip solution photo card reader

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